

**IN THE CLAIMS:**

1. (Currently Amended) A method for fabricating an ultra-shallow surface channel MOS transistor, the method comprising:  
forming CMOS source and drain regions, and an intervening well region with a surface;  
depositing a metal oxide surface channel on the surface overlying the well region, selected from the group of materials including indium oxide ( $\text{In}_2\text{O}_3$ ), ZnO, RuO, ITO, and  $\text{La}_{1-x}\text{Sr}_x\text{CoO}_3$ ;  
forming a high-k dielectric, having a thickness in the range of 1 to 5nm, overlying the surface channel; and,  
forming a gate electrode overlying the high-k dielectric.
- 2-3. Canceled
4. (Previously Presented) A method for fabricating an ultra-shallow surface channel MOS transistor, the method comprising:  
forming CMOS source and drain regions, and an intervening well region with a surface;  
depositing a surface channel on the surface overlying the well region;  
forming a high-k dielectric overlying the surface channel;  
depositing a placeholder material overlying the surface channel;  
conformally depositing oxide;

etching the placeholder material to form a gate region overlying the surface channel; and,  
forming a gate electrode overlying the high-k dielectric in the gate region.

5. (Original) The method of claim 4 further comprising:

following the deposition of the placeholder material, lightly doped drain (LDD) processing the source and drain regions;

wherein forming a high-k dielectric insulator overlying the surface channel includes depositing the high-k dielectric prior to the deposition of the placeholder material;

the method further comprising:

forming sidewall insulators adjacent the surface channel, high-k dielectric insulator, and gate region; and,

heavy ion implanting and activating the source and drain regions.

6. (Original) The method of claim 4 further comprising:

prior to the deposition of the surface channel, lightly doped drain (LDD) processing the source and drain regions;

heavy ion implanting and activating the source and drain regions; and,

wherein forming a high-k dielectric insulator overlying the surface channel includes depositing the high-k dielectric following the etching of the placeholder material to form the gate region.

7. (Previously Presented) A method for fabricating an ultra-shallow surface channel MOS transistor, the method comprising:  
forming CMOS source and drain regions, and an intervening well region with a surface;  
depositing a metal oxide surface channel on the surface overlying the well region having a thickness in the range of 10 to 20 nanometers (nm);  
forming a high-k dielectric overlying the surface channel;  
and,  
forming a gate electrode overlying the high-k dielectric.

8. (Previously Presented) A method for fabricating an ultra-shallow surface channel MOS transistor, the method comprising:  
forming CMOS source and drain regions, and an intervening well region with a surface;  
depositing a metal oxide surface channel on the surface overlying the well region having a resistivity in the range between 0.1 and 1000 ohm-cm;  
forming a high-k dielectric overlying the surface channel;  
and,  
forming a gate electrode overlying the high-k dielectric.

9. (Original) The method of claim 1 wherein forming a high-k dielectric insulator overlying the surface channel includes depositing a high-k dielectric material selected from the group including  $\text{HfO}_2$ ,  $\text{HfAlO}_x$ ,  $\text{ZrO}_2$ , and  $\text{Al}_2\text{O}_3$ .

10. Canceled

11. (Original) The method of claim 4 wherein depositing a placeholder material overlying the surface channel includes forming placeholder material to a first thickness with a placeholder material surface; and,

wherein conformally depositing oxide includes depositing oxide to a second thickness in the range of 1.2 to 1.5 times the first thickness; and,

the method further comprising:

chemical mechanical polishing (CMP) the oxide to the level of the placeholder material surface.

12. (Original) The method of claim 5 wherein forming sidewall insulators adjacent the surface channel, high-k dielectric insulator, and gate region includes forming sidewalls from a material selected from the group including  $\text{Si}_3\text{N}_4$  and  $\text{Al}_2\text{O}_3$ .

13. (Currently Amended) An ultra-shallow surface channel MOS transistor, the transistor comprising:  
a source region;  
a drain region;  
a well region intervening between the source and drain with a surface;

a metal oxide surface channel overlying the well region,  
selected from a group of materials including indium oxide ( $\text{In}_2\text{O}_3$ ),  $\text{ZnO}$ ,  
 $\text{RuO}$ ,  $\text{ITO}$ , and  $\text{La}_{1-x}\text{Sr}_x\text{CoO}_3$ ;

a high-k dielectric insulator, having a thickness in the range  
of 1 to 5 nm, overlying the surface channel; and,

a gate electrode overlying the high-k dielectric layer.

14-15. Canceled

16. (Previously Presented) An ultra-shallow surface  
channel MOS transistor, the transistor comprising:

a source region;

a drain region;

a well region intervening between the source and drain with  
a surface;

a surface channel overlying the well region;

a high-k dielectric insulator overlying the surface channel;

a placeholder overlying the surface channel, forming a  
temporary gate region; and,

a gate electrode overlying the high-k dielectric layer, formed  
in the gate region.

17. (Original) The transistor of claim 16 wherein the  
placeholder is temporarily formed directly overlying the high-k dielectric  
insulator;

the transistor further comprising:

sidewall insulators adjacent the surface channel, high-k dielectric insulator, and the gate region.

18. (Original) The transistor of claim 16 wherein the placeholder is temporarily formed directly overlying the surface channel.

19. (Previously Presented) An ultra-shallow surface channel MOS transistor, the transistor comprising:

- a source region;
- a drain region;
- a well region intervening between the source and drain with a surface;
- a metal oxide surface channel overlying the well region having a thickness in the range in the range of 10 to 20 nanometers (nm);
- a high-k dielectric insulator overlying the surface channel;

and

- a gate electrode overlying the high-k dielectric layer.

20. (Previously Presented) An ultra-shallow surface channel MOS transistor, the transistor comprising:

- a source region;
- a drain region;
- a well region intervening between the source and drain with a surface;
- a metal oxide surface channel overlying the well region having a resistivity in the range between 0.1 and 1000 ohm-cm;

a high-k dielectric insulator overlying the surface channel;  
and  
a gate electrode overlying the high-k dielectric layer.

21. (Original) The transistor of claim 13 wherein the high-k dielectric insulator is a material selected from the group including HfO<sub>2</sub>, HfAlO<sub>x</sub>, ZrO<sub>2</sub>, and Al<sub>3</sub>O<sub>4</sub>.

22. Canceled

23. (Original) The transistor of claim 17 wherein the sidewall insulators are a material selected from the group including Si<sub>3</sub>N<sub>4</sub> and Al<sub>2</sub>O<sub>3</sub>.